MINEWSEMI

LoRa Module
ME21LS1A



Datasheet

V 1.0.1

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Version Note

Version	Details	Contributor(s)	Date	Notes
1.0.0	First edit	Vincle	2026.08.25	

Part Number

Model	Hardware Code
ME21LS1A	-

Note: The meaning of "X"	
	0 AS923, Support 923MHz frequency 1 AU915, Support 915-928MHz frequency 2 CN470, Support 470-510MHz frequency 3 CN779, Support 779-787MHz frequency 4 EU433, Support 433MHz frequency 5 EU868, Support 863-870MHz frequency 6 IN865, Support 865-867MHz frequency 7 KR920, Support 920-923MHz frequency 8 RU864, Support 864-870MHz frequency 9 US915, Support 902-928MHz frequency

The marking on the product's shielding cover is subject to change based on certification updates.
The actual marking on the shielding cover at the time of shipment shall prevail.

Please be aware that changes in the marking do not affect product performance or usage; therefore, no separate notification will be issued regarding such changes.

For customization requests, please contact MinewSemi's sales team for confirmation.

*Due to the limited module size, regulatory marks and certification IDs are provided in this datasheet and/or on the packaging. The final product incorporating this module shall include a label indicating that it contains a certified module.

Click the icon to view and download the latest product documents electronically.
https://en.minewsemi.com/file/ME21LS1A_Datasheet_K_EN.pdf

ME21LS1A-LLCC68/SX1262

High-power, Ultra-long-range, Small-size, High-sensitivity LoRa Module

The ME21LS1A module is a LoRa wireless half-duplex transceiver module based on Semtech's LLCC68/SX1262. It supports global ISM frequency bands and features high transmit power, ultra-long range, and a compact design with an easy-to-use SPI interface.

With enhanced transmit power, the module integrates a high-efficiency power amplifier to provide up to +29 dBm transmit power. It also offers high receiver sensitivity, down to -146 dBm. The module complies with the physical layer requirements of the LoRaWAN® standard and supports LoRa® P2P (Point-to-Point) communication, enabling customers to quickly establish private long-range LoRa® networks.

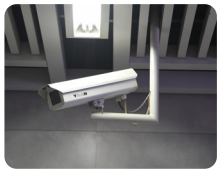
FEATURES

- No integrated MCU: An external MCU is required and controls the module through the SPI interface.
- Programmable data rate: Supports data rates of up to 62.5 kbps for both LoRa and FSK modulation.
- Extended communication range
- SPI interface: Can be directly connected to various MCUs for easy integration.

KEY PARAMETERS

ME21LS1A			
Chip Model	LLCC68/SX1262	**Antenna**	U.FL/ANT PIN
Module Size	16.4x15x3mm	**GPIO**	-
Receiving Sensitivity	SX1262: -146dBm LLCC68: -126dBm	**Transmission Power**	LoRa: +29dBm
Current(TX)	700mA@avg.	**Current(RX)**	12.25mA

APPLICATIONS



Security and alarm systems



Agricultural sensors



Instrumentation and smart metering



Building automation



Smart cities

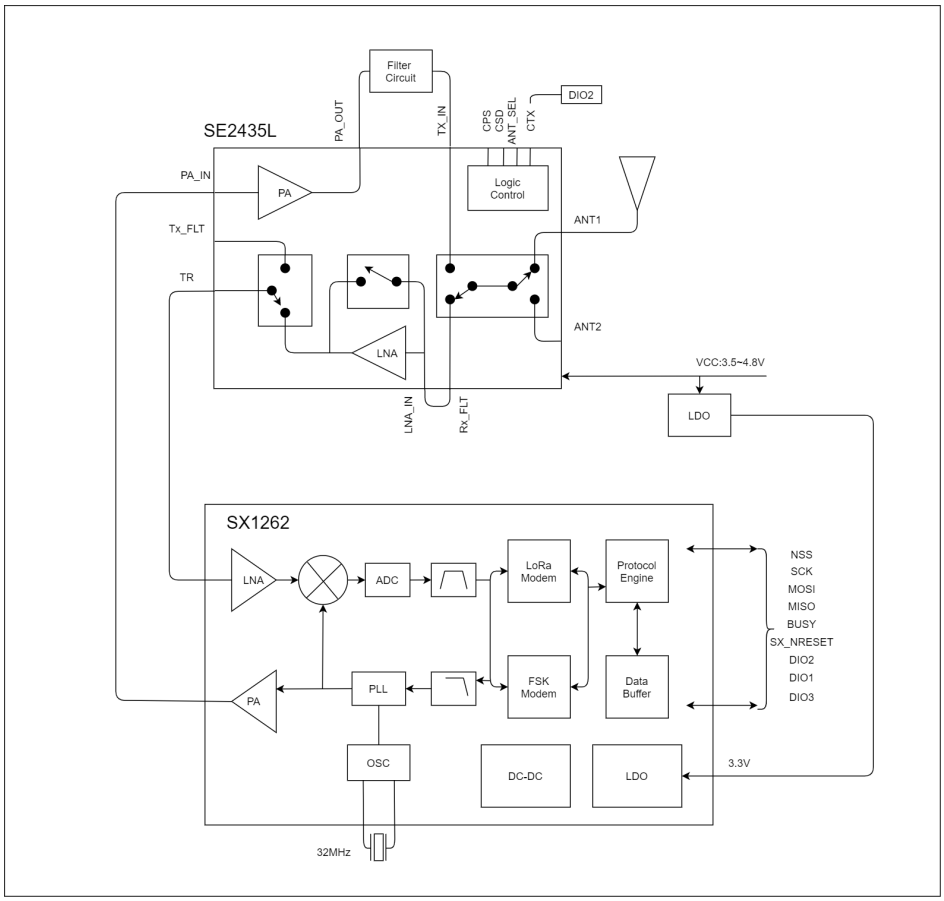
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1 BLOCK DIAGRAM

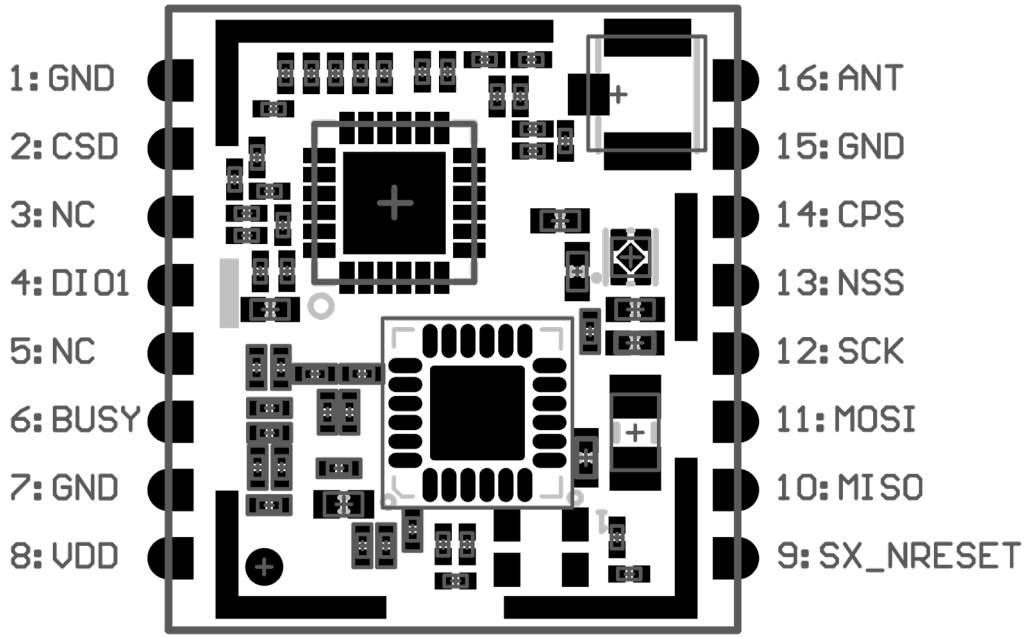


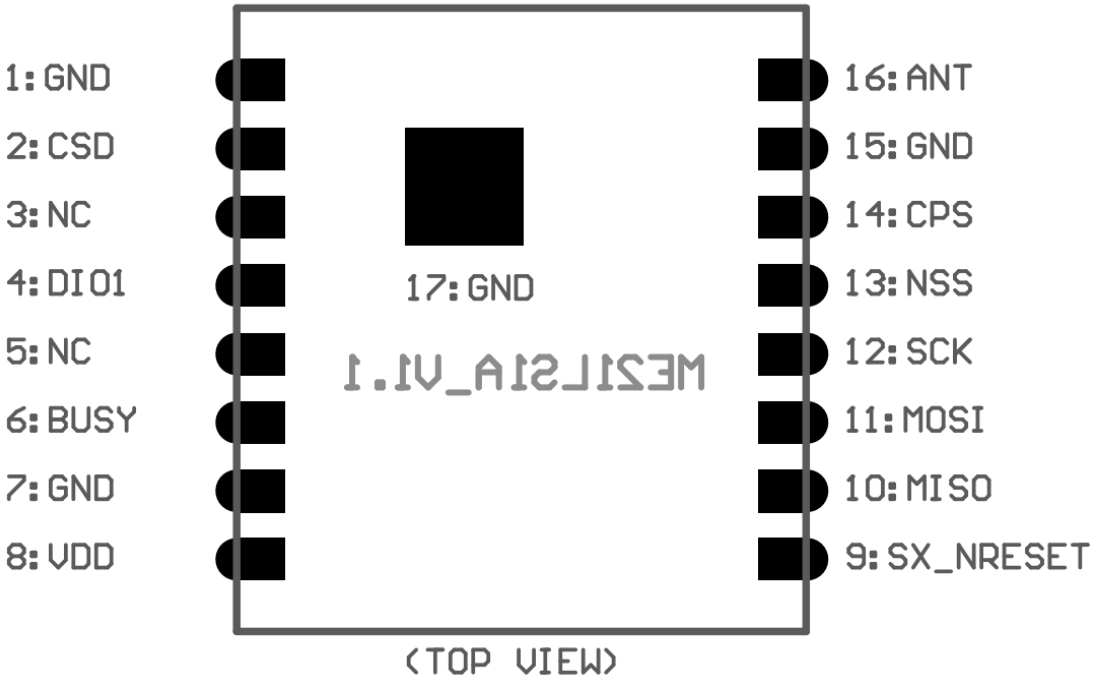
2 ELECTRICAL SPECIFICATION

Parameter	Value	Notes
Operating Voltage	3.5V-4.8V	Standard voltage 4.0V
Working Temperature	-40℃~+85℃	Storage temperature is -40℃~+125℃
Operating Frequency	915MHz	Optional 868MHz frequency bands, Default set is 915MHz
Transmission Power	+29dBm	Configurable
Current(RX)	12.25mA	RX mode
Current(TX)	700mA	TX mode avg. value
Module Dimension	16.4*15*3mm	

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3 PIN DESCRIPTION



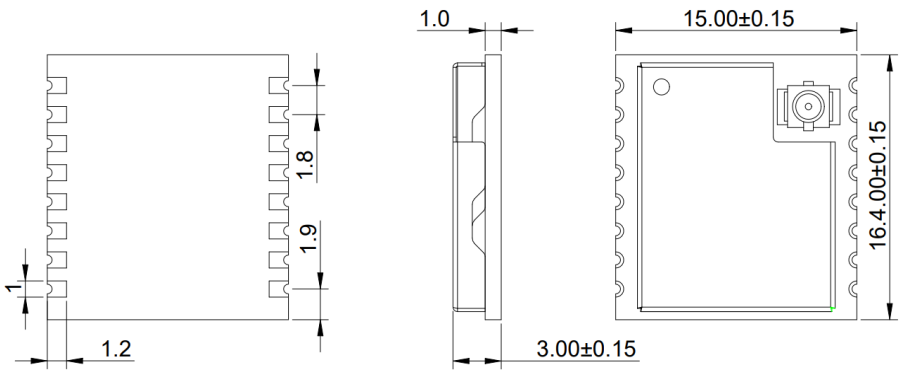


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4 PIN DEFINITION

Number	Symbol	Type	Definition	Notes
1	GND	-	Grounded	
2	CSD	SWITCH	Control	
3	NC	-	Empty pin	
4	DIO1	I/O	Multi-functional digital I/O port	
5	NC	-	Empty pin	
6	BUSY	O	Busy indicator pin	
7	GND	-	Grounded	
8	VDD	I	Positive power supply	Power supply is 3.5V - 4.8V, Standard voltage is 4.0V
9	SX_NRESET	I/O	Reset signal	Active low level
10	MISO	O	SPI slaver output	
11	MOSI	I	SPI slave input	
12	SCK	I	SPI Clock	
13	NSS	I	SPI slave chips select	
14	CPS	SWITCH	Control	
15	GND	-	Grounded	
16	ANT	-	Antenna connect pin	
17	GND	-	Grounded	

5 MECHANICAL DRAWING

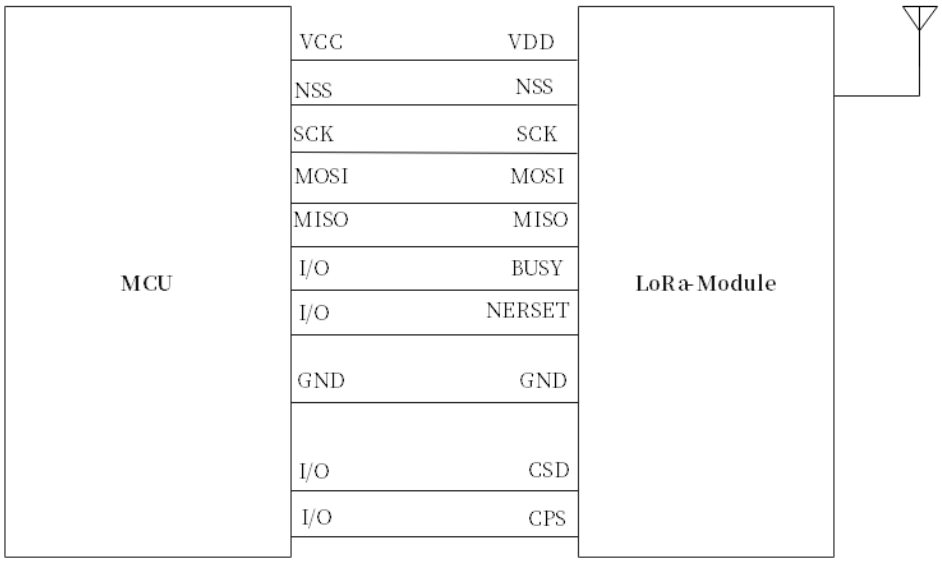


Default unit: mm Default tolerance: ±0.15

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6 MODULE CONNECTION DESCRIPTION

6.1 Connection Diagram



6.2 Power Supply

The module operates within a supply voltage range of 3.5 V to 4.8 V. For proper operation, the recommended standard supply voltage is 4.0 V.

6.3 SPI Interface Characteristics

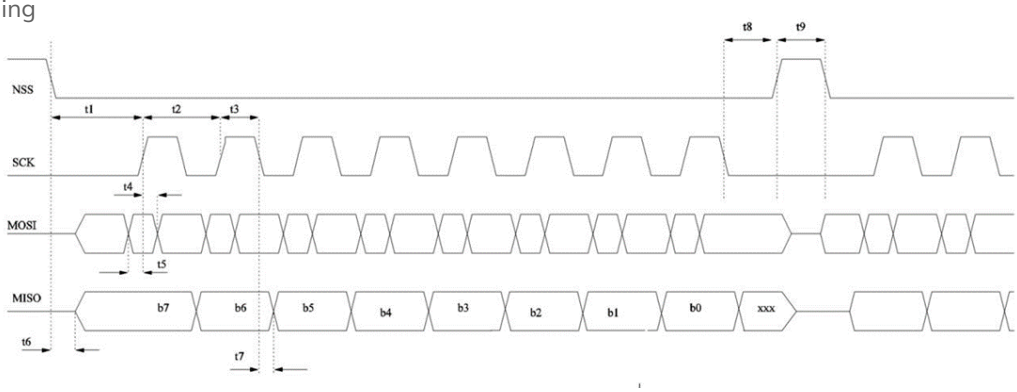
The SPI interface operates with an external SCK clock and supports a clock rate of up to 16 MHz.
Data transmission starts when the NSS pin is pulled low. When the NSS pin is high, MISO is in a high-impedance state.
SPI Timing Requirements (The chip supports Slave mode only.)

Symbol	Description	Minimum	Typical	Maximum	unit
t1	NSS falling edge to SCK setup time	32	-	-	ns
t2	SCK period	62.5	-	-	ns
t3	SCK high time	31.25	-	-	ns
t4	MOSI to SCK hold time	5	-	-	ns
t5	MOSI to SCK setup time	5	-	-	ns
t6	MOSI to SCK setup time	0	-	15	ns
t7	SCK falling to MISO delay	0	-	15	ns
t8	SCK to NSS rising edge hold time	31.25	-	-	ns
t9	NSS high time	125	-	-	ns

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Symbol	Description	Minimum	Typical	Maximum	unit
t10	NSS falling edge to SCK setup time when switching from SLEEP to STDBY_RC mode	100	-	-	s
t11	NSS falling to MISO delay when switching from SLEEP to STDBY_RC mode	0	-	150	s

Active Timing



6.3.1 DIO and IRQ Control

The following commands are used to configure the IRQs and DIOs of the control chip. At least one DIO must be assigned for IRQ, and the BUSY line is also mandatory.

Command	Operate code	Parameters	Description
SetDioIrqParams	0x08	IrqMask[15:0], Dio1Mask[15:0], Dio2Mask[15:0], Dio3Mask[15:0],	Configure the IRQ and DIOs for each IRQ
GetIrqStatus	0x12	-	Get the values of the triggered IRQs
ClearIrqStatus	0x02	-	Clear one or several of the IRQs
SetDIO2AsRfSwitchCtrl	0x9D	Enable	Configure DIO2 to control the RF switch
SetDIO3AsTcxoCtrl	0x97	tcxoVoltage, timeout[23:0]	Configure DIO3 to control the TCXO

6.3.2 Module TX/RX Mode Control

MODE	CPS	CSD	CTX
Sleep(all off)	0	0	0
Receiver or transmit bypass	0	1	0
Receiver LNA mode	1	1	0
Transmit	X	1	1

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Any of the 3 DIOs can be selected as an output interrupt source for the application. When the application receives an interrupt, it can determine the source by using the command GetIrqStaus(...). The interrupt can then be cleared using the ClearIraqStaus(...) command. The pin description is as fllows:

(1) DIO1 is the general-purpose IRQ line, any interrupt can be mapped to DIO1. The complete list of available IRQ can be found in Section 8.4 “Digital Interface Status and Chip Modes” on page 55 in the chip datasheet.
(2) DIO2 has a dual function. As DIO1, DIO2 can be used as a general-purpose IRQ line and any IRQ can be routed through this pin. Also, DIO2 can be configured to drive an RF switch through the use of the command SetDio2ASRfSwitchCtrl(..). In this mode, DIO2 will be at a logical 1 during Tx and at a logical 0 in any other mode.DIO2 is internally connected to the TCXO by default.
(3) DIO3 also has a dual function and as DIO1 or DIO2, it can be as a general-purpose IRQ line, Also, DIO3 can be used to automatically control a TCXO through the command SetDio3AsTCXOCtrl(...). In this mode, the device automatically enables the TCXO when required.

> ⚠ Note: For the SX1262, the configured transmit power must not exceed 10 dBm, otherwise the PA component may be damaged.

6.3.3 Module Voltage and Power Table

The module transmit power was tested at 915MHz, SF7@125KHz. The following table shows the measured power performance:

Module Voltage	SX1262 Power	Avg Power(dBm)	Avg Current(A)
3.6V	5	27.2	0.60
	9	27.6	0.64
4V	5	28.1	0.67
	9	28.3	0.70
4.5V	5	28.9	0.74
	9	29.1	0.76
4.8V	5	29.0	0.76
	9	29.7	0.80

6.3.4 Module Power Consumption Specification

The following power consumption tests were conducted at a supply voltage of 4.4V under room temperature conditions. The measurements were performed in the 915 MHz frequency band.
In TX mode, with a 1-second transmission interval, the power consumption is as follows: (TX bandwidth: 125 kHz, TX output power: +29dBm)

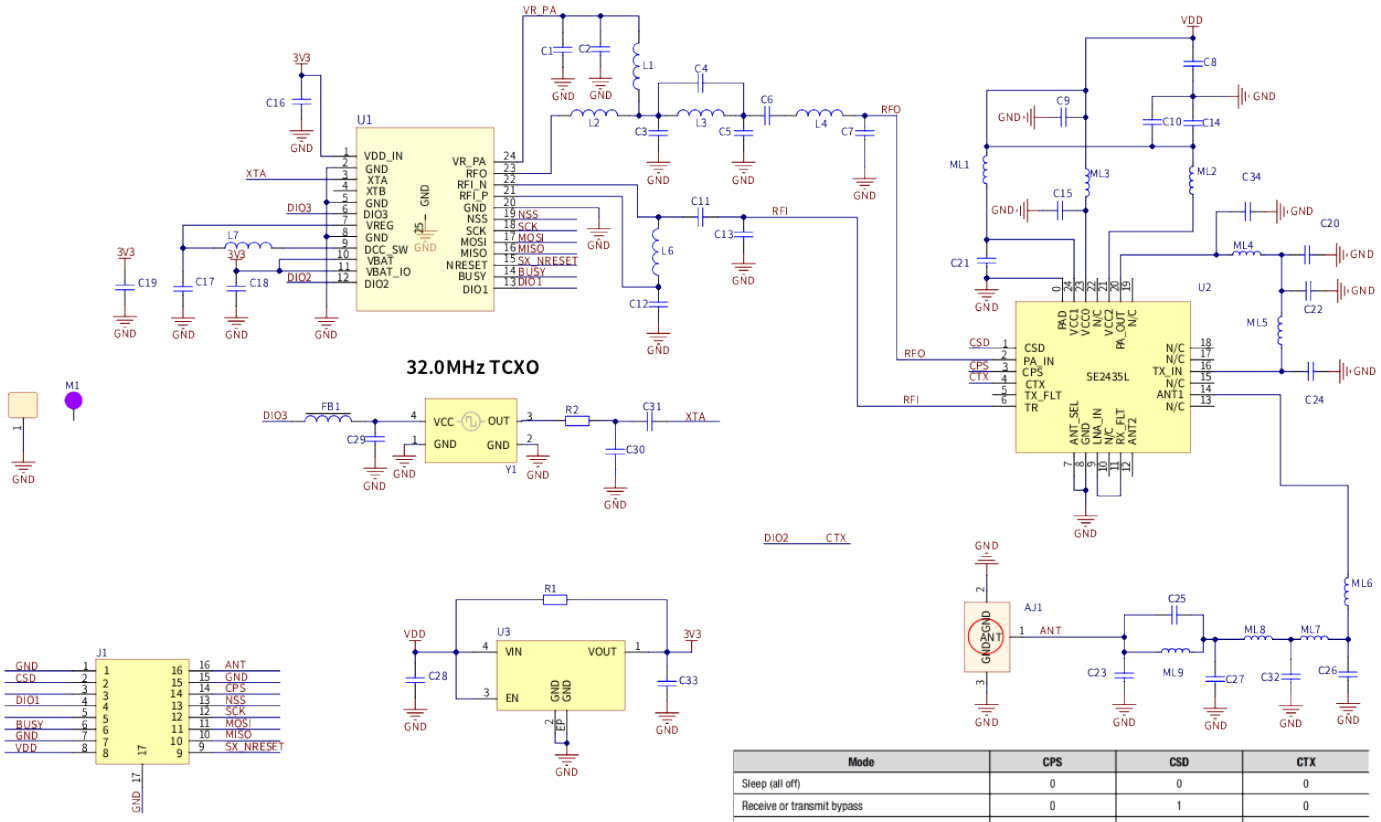
Status \ Power	SF Mode	Peak	Avg
TX	SF7	930mA	36.93mA

In RX mode, the power consumption is as follows: (RX bandwidth: 125kHz, TX output power: +29dBm)

Status \ Power	SF Mode	Peak	Avg
RX	SF7	13.25mA	12.25mA

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7 ELECTRICAL SCHEMATIC



Mode	CPS	CSD	CTX
Sleep (all off)	0	0	0
Receive or transmit bypass	0	1	0
Receive LNA mode	1	1	0
Transmit	X	1	1

Any of the 3 DIOs can be selected as an output interrupt source for the application. When the application receives an interrupt, it can determine the source by using the command *GetIrqStatus(...)*. The interrupt can then be cleared using the *ClearIrqStatus(...)* command. The Pin Description is as follows:

DIO1 is the generic IRQ line, any interrupt can be mapped to DIO1. The complete list of available IRQ can be found in Section 8.4 "Digital Interface Status versus Chip modes" on page 55.

DIO2 has a double functionality. As DIO1, DIO2 can be used as a generic IRQ line and any IRQ can be routed through this pin. Also, DIO2 can be configured to drive an RF switch through the use of the command *SetDio2AsRfSwitchCtrl(...)*. In this mode, DIO2 will be at a logical 1 during Tx and at a logical 0 in any other mode.

DIO3 also has a double functionality and as DIO1 or DIO2, it can be used as a generic IRQ line. Also, DIO3 can be used to automatically control a TCXO through the command *SetDio3AsTCXOCtrl(...)*. In this case, the device will automatically power cycle the TCXO when needed.

> * Note: If you need a different LoRa frequency band solution, please contact the sales representative.

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8 PCB DESIGN

8.1 Disclaimer

This document is provided as a recommended design reference for wireless modules and does not constitute any explicit or implied guarantee of performance or compliance. Due to differences in PCB layout, enclosure structure, antenna selection, and application environments of the end product, this document cannot guarantee RF performance in all scenarios. Users must conduct sufficient RF performance and compliance verification after completing the final product design and shall bear full responsibility for design and application outcomes. Our company reserves the right to modify the contents of this document without prior notice.

8.2 Core Rules for Module Placement

Board Edge Priority Rule

The RF output/antenna side of the module must face the edge of the main PCB to ensure that antenna radiation is directed outward from the board without obstruction. Placing the module in a closed central area of the PCB is strictly prohibited.

Keep-Out Area Rule

A 0.5 mm area around the module body must be kept clear. Non-ground components and non-ground signal traces are prohibited within this area. Within 4 mm around the RF side of the module, copper pours, unrelated components, and non-RF signal traces are strictly prohibited.

Interference Isolation Rule

The module must maintain a minimum safe distance from strong interference sources. Adjacent placement on the same layer is prohibited. Isolation using different PCB layers and shielding covers is recommended. General isolation requirements are as follows:

Interference Source Type	Minimum Recommended Isolation Distance
DC-DC switching power supplies, power inductors, power transformers	20mm
USB 3.0 / HDMI 2.0 / DDR / High-speed SDIO interfaces	20mm
MCU high-frequency clock circuits, Ethernet PHY chips	15mm
Displays, cameras, FPC cables with wiring	25mm

Structural Clearance Rule

The minimum distance between the module and metal screws, clips, standoffs, and other structural parts must be ≥5 mm. At least 4 mm of SMT soldering and rework clearance must be reserved around the module. The RF side of the module must not be enclosed inside a fully metal cavity.

Multiple Modules on the Same PCB

When placing multiple wireless modules of the same or different types on the same PCB, the minimum spacing between modules must be ≥50 mm to avoid mutual interference.

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8.3 GENERAL PCB DESIGN REQUIREMENTS

Grounding Design

The main PCB must maintain a complete and continuous ground plane. Splitting the ground plane within the module projection area or RF surrounding area is strictly prohibited. All module ground pins must be soldered. At least one grounding via should be placed near each ground pad and connected to the main ground plane. A complete ground plane with dense grounding vias may be placed under the non-RF area of the module to improve shielding performance.

Power Supply Design

Decoupling capacitor combinations must be placed close to the module power input pins. The trace length between capacitor pads and power pins should be ≤0.5 mm, and at least two grounding vias should be placed near the ground terminal. For switching power supply applications, a π-type filter circuit footprint must be reserved near the module power input pins.

RF Trace Design

The entire RF path must maintain a strict 50 Ω characteristic impedance (tolerance ±10%). RF traces should be as short as possible and routed preferably in straight lines. Sharp or right-angle corners are prohibited; curved routing with a radius ≥3 times the trace width is recommended. Branch traces and stub traces are prohibited. A continuous reference ground plane must exist beneath the RF traces, and no other signal traces should be routed within 3 times the trace width on either side. Ground shielding should be applied throughout the RF routing.

Control Interface Design

Control signal traces such as UART, SPI, and I2C should be routed away from RF areas with short and simple routing paths and continuous ground shielding. Parallel routing adjacent to RF traces is prohibited. ESD protection devices must be placed close to external PCB connectors and must not be placed near module pins.

Footprint Design

Strictly use the standard PCB footprint provided by our company. Unauthorized modification of pad size or spacing is prohibited to ensure soldering reliability.

8.4 DESIGN RESTRICTIONS

Do not place the RF side of the module facing the inside of the PCB or away from the board edge.

Do not place copper pours, components, or fully enclosed metal housings without openings over the antenna area.

Do not route RF traces across split ground planes, without a complete reference ground, or with right-angle corners.

Do not place modules adjacent to strong interference sources or split the ground plane in the module area.

Do not leave module ground pins unconnected or inadequately grounded.

8.5 MODULE PLACEMENT EXAMPLE

For end products, antenna position significantly affects overall system performance. The module should preferably be placed at the edge or corner of the PCB to maximize the clearance area and reduce interference from surrounding components. The PCB area directly beneath the module antenna should be hollowed out to keep the antenna region suspended, while no signal traces, metal objects, or other interference sources should exist within 3–5 mm around the antenna area. The figure below demonstrates an example of proper module placement on the main PCB for optimal RF performance. The first recommended layout method should be used whenever possible, as the module antenna design has been tuned and optimized based on this configuration.

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Correct Example

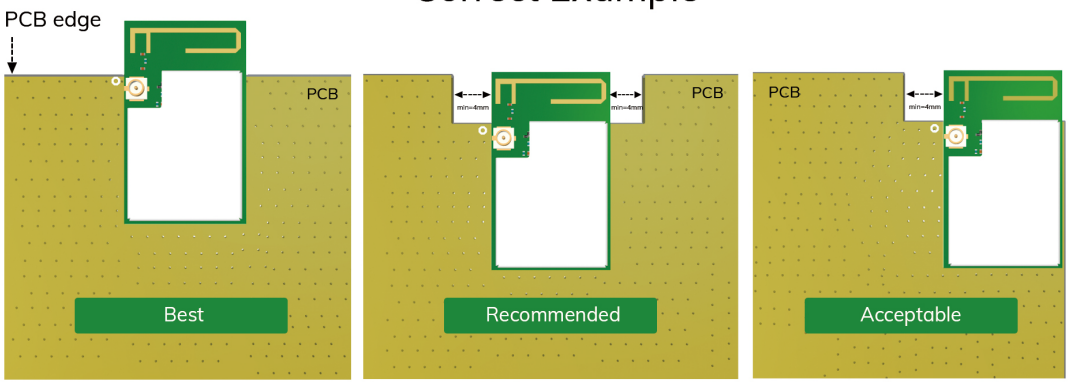


Figure 1 Figure 2 Figure 3

Incorrect Example

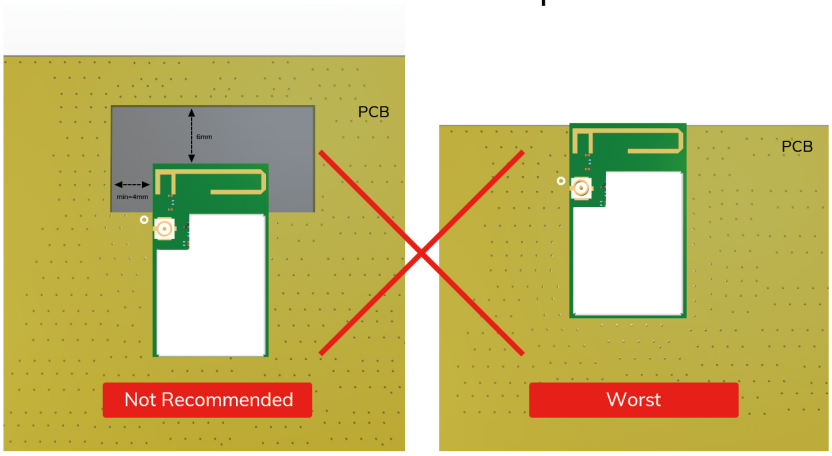
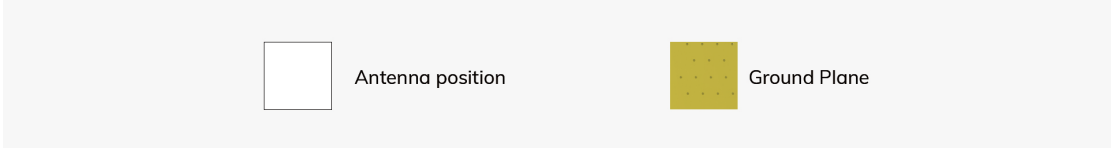


Figure 4 Figure 5



9 DIFFERENCE BETWEEN SX1262 AND LLCC68

9.1 Spreading Factor (SF)

SX1262 LoRa SF = SF5-SF12, BW=7.8-500KHz
LLCC68 LoRa SF = 5 - 6 - 7 - 8 - 9, BW=125KHz
LoRa SF = 5 - 6 - 7 - 8 - 9 - 10, BW=250KHz
LoRa SF = 5 - 6 - 7 - 8 - 9 - 10 - 11, BW=500KHz

9.2 LoRaWAN DR

SX1262 LoRaWAN DR: Supports all DR0-DR5
LLCC68 LoRaWAN DR: Does not support DR0@SF12/125kHz, DR1@SF11/125kHz, DR2@SF10/125kHz
Therefore, for the LLCC68, the network should generally be configured not to switch nodes to DR0, DR1, or DR2.

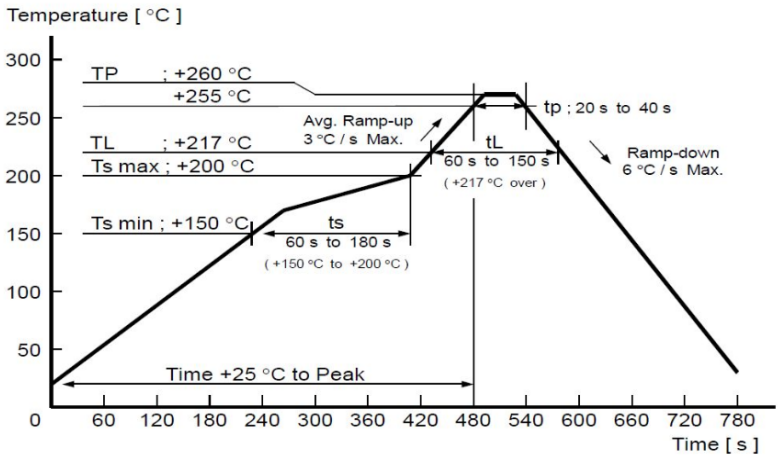
9.3 LoRaWAN ADR

SX1262: LoRaWAN ADR: Unrestricted; full-range adaptive
LLCC68: LoRaWAN ADR: Restricted to SF7/SF8/SF9

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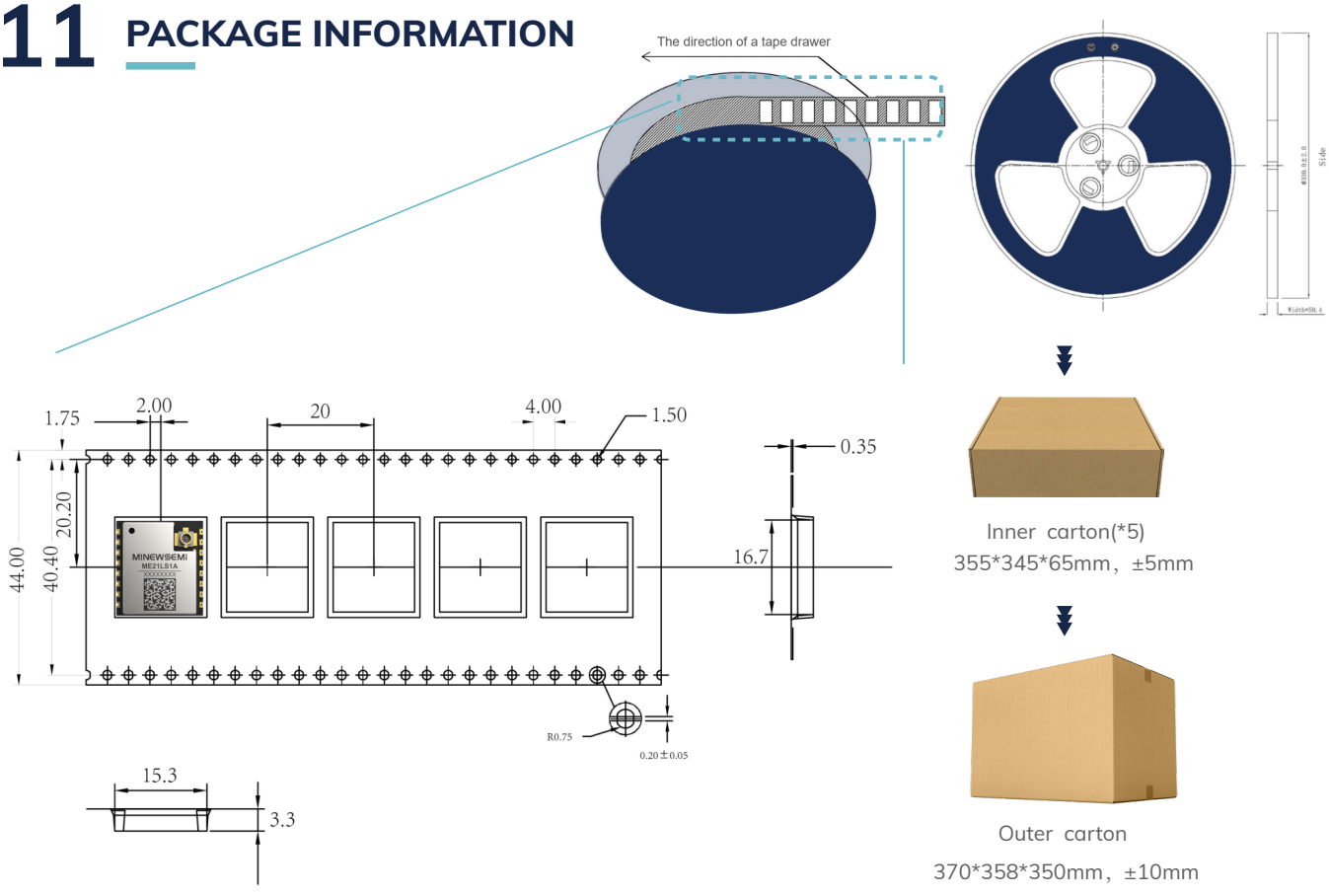
10 REFLOW AND SOLDERING

1) Perform SMT according to the reflow oven temperature profile provided below, with a maximum temperature of 260°C;
2) Follow IPC/JEDEC standards; Peak temperature: < 260°C; Number of reflows: ≤2 times; For SMT involving double-sided placement, it is recommended that the module side undergoes reflow soldering only once. For any special processes, please contact our company.



3) For module SMT, it is recommended to create a localized stepped stencil with a thickness of 0.2mm, followed by an outward extension of 0.8mm.
4)After opening, if the entire package is not used at once, it should be stored in a vacuum to prevent long-term exposure to air, which can cause moisture absorption and pad oxidation. If there is a gap of 7 to 30 days before reuse, it is recommended to bake the tape at 65-70°C for 24 hours without unrolling it before returning to SMT.
5) ESD protection measures should be implemented before using SMT.

11 PACKAGE INFORMATION



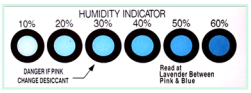
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Remarks

General material list for FCL packaging:



Carrier tape packaging tray



Humidity Indicator
(1 pcs/bag)



Desiccant
(placed in a vacuum bag)



Vacuum bag



Inner carton(*5)
355*345*65mm，±5mm



Outer carton
370*358*350mm，±10mm

Other:

Moisture-proof label (attached to the vacuum bag)

Certification label (attached to the vacuum bag)

Outer box label

Default unit：mm Default tolerance：±0.1

Packing Detail	Specification	Net Weight	Gross Weight	Dimension
ME21LS1A	850pcs	1759.5g	2299.5g	W=44mm，T=0.35mm

Note: Default weight tolerance all are within 10g（except the special notes）

12 STORAGE CONDITIONS

- **Please use this product within 6 months after signing the receipt.**
  - This product should be stored without opening the package at an ambient temperature of 5~35°C and a humidity of 20~70%RH.
  - This product should be left for more than 6 months after receipt and should be confirmed before use.
  - The product must be stored in a non-corrosive gas (Cl2, NH3, SO2, NOx, etc.).
  - To avoid damaging the packaging material, do not apply any excessive mechanical shocks, including but not limited to sharp objects adhering to the packaging material and product dropping.

- **This product is suitable for MSL2 (based on JEDEC standard J-STD-020).**
  - After opening the package, the product must be stored at ≤30°C/<60%RH. It is recommended to use the product within 3-6 months after opening the package.
  - When the color of the indicator in the package changes, the product should be baked before welding.

- **Baking is not required for one year if exposure is limited to <30°C and 60%RH. Refer to MSL2 for exposure criteria for moisture sensitivity level. If exposed to (≥168h@85°C/60%RH) conditions or stored for more than one year, recommended baking conditions.**

  1. 120 +5/-5°C, 8 hours, 1 time

  Products must be baked individually on heat-resistant trays because the materials (base tape, reel tape, and cover tape) are not heat-resistant, and the packaging material may be deformed at temperatures of 120℃;

  2、90℃ +8/-0℃，24hours，1times

  The base tape can be baked together with the product at this temperature. Please pay attention to the uniformity of heat.

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13 HANDLING CONDITIONS

- Be careful in handling or transporting products because excessive stress or mechanical shock may break products.
- Handle with care if products may have cracks or damages on their terminals. If there is any such damage, the characteristics of products may change. Do not touch products with bare hands that may result in poor solder ability and destroy by static electrical charge.

14 QUALITY

Cognizant of our commitment to quality, we operate our own factory equipped with state-of-the-art production facilities and a meticulous quality management system. We hold certifications for ISO9001, ISO14001, ISO27001, OHSA18001, BSCI.

Every product undergoes stringent testing, including transmit power, sensitivity, power consumption, stability, and aging tests. Our fully automated module production line is now in full operation, boasting a production capacity in the millions, capable of meeting high-volume production demands.

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16 RELATED DOCUMENTS

- MinewSemi_Product_Naming_Reference_Manual
  https://en.minewsemi.com/file/MinewSemi_Product_Naming_Reference_Manual_EN.pdf
- MinewSemi_Connectivity_Module_Catalogue
  https://en.minewsemi.com/file/MinewSemi_Connectivity_Module_Catalogue_EN.pdf

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